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1   A unified framework for race analysis of asynchronous networks   92%

J. A. Brzozowski , C.-J. Seger
Journal of the ACM (JACM) January 1989
Volume 36 Issue 1

> A unified framework is developed for the study of asynchronous circuits of both gate and MOS type. A basic network model consisting of a directed graph and a set of vertex excitation functions is introduced. A race analysis model, using three values (0, 1, and x), is developed for studying state transitions in the network. It is shown that the results obtained using this model are equivalent to those using ternary simulation. It is also proved that the set of state variables can be reduced ...

2   Mapping switch-level simulation onto gate-level hardware accelerators   85%

Alok Jain , Randal E. Bryant
Proceedings of the 28th conference on ACM/IEEE design automation conference June 1991

3   Transistor level test generation for MOS circuits   84%

Madhukar K. Reddy , Sudhakar M. Reddy , Prathima Agrawal
Proceedings of the 22nd ACM/IEEE conference on Design automation June 1985

> Due to inaccuracies in gate level models of VLSI digital circuits, current practice is to use transistor level simulators to analyze VLSI digital circuits. The inaccuracies of gate level models are even more severe when faults in digital circuits are considered. For this reason, recently several researchers have proposed the use of test pattern generation from digital circuits described at the transistor level. In this paper an efficient test pattern generation procedure for digital circuit ...

4   Analysis of cyclic combinational circuits   84%

Sharad Malik
Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design
November 1993

5   Formal hardware verification by symbolic ternary trajectory evaluation   84%

Randal E. Bryant , Derek L. Beatty , Carl-Johan H. Seger
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1 **Stability analysis and stabilizing control synthesis via Lyapunov's second method directly on bond graphs of nonlinear systems**
Junco, S.;
Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on , 15-19 Nov. 1993
Page(s): 2065 -2069 vol.3

[Abstract]   [PDF Full-Text (324 KB)] **IEEE CNF**

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2 **Design, simulation, and validation of a bond graph model and controller to switch between pump and motor operation using four on/off valves with a hydraulic axial piston pump/motor**
Lumkes, J.H., Jr.; Fronczak, F.J.;
American Control Conference, 2000. Proceedings of the 2000 , Volume: 5 , 28-30 June 2000
Page(s): 3605 -3609 vol.5

[Abstract]   [PDF Full-Text (404 KB)] **IEEE CNF**

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3 **PCC: a modeling technique for mixed control/data flow systems**
Grotker, T.; Schoenen, R.; Meyr, H.;
European Design and Test Conference, 1997. ED&TC 97. Proceedings , 17-20 March 1997
Page(s): 482 -486

[Abstract]   [PDF Full-Text (552 KB)] **IEEE CNF**

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4 **Expansionist/context-sensitive methodology: engineering of complex adaptive systems**
Clymer, J.R.;
Aerospace and Electronic Systems, IEEE Transactions on , Volume: 33 Issue: 2 , April 1997

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Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific , 25-28 Jan. 2000
Page(s): 43 -48

[Abstract]   [PDF Full-Text (524 KB)] **IEEE CNF**

2 **Essential issues for IP reuse**
Gajski, D.D.; Wu, A.C.-H.; Chaiyakul, V.; Mori, S.; Nukiyama, T.; Bricaud, P.;
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[Abstract]   [PDF Full-Text (376 KB)] **IEEE CNF**

3 **Clock-driven performance optimization in interactive behavioral synthesis**
Hsiao-Ping Juan; Gajski, D.D.; Chaiyakul, V.;
Computer-Aided Design, 1996. ICCAD-96. Digest of Technical Papers., 1996 IEEE/ACM International Conference on , 10-14 Nov. 1996
Page(s): 154 -157

[Abstract]   [PDF Full-Text (404 KB)] **IEEE CNF**

4 **Condition Graphs For High-quality Behavioral Synthesis**
Hsiao-ping Juan; Chaiyakul, V.; Gajski, D.D.;
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Page(s): 170 -174

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5 **An algorithm for array variable clustering**
Ramachandran, L.; Gajski, D.D.; Chaiyakul, V.;
European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings. , 28 Feb.-3 March 1994
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6 Accurate layout area and delay modeling for system level design

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2 **A new algorithm for the binate covering problem and its application to the minimization of Boolean relations**
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3 **Exact dichotomy-based constrained encoding**
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4 **Expressing and implementing operational profiles for reactive software validation**
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14 Compact thermal models of packages used in conduction cooled applications
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